G-LINK

GLT41316

64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE

June 1998 (Rev 2)

Features :

- 65,536 words by 16 bits organization.
- Fast access time and cycle time.
- Dual $\overline{WE}$ Input.
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 256 refresh cycles per 4ms.
- Available in 40-pin 400 mil SOJ,and 40/44 pin TSOP (II).
- Single 5.0V±10% Power Supply.
- All inputs and Outputs are TTL compatible.
- Fast Page Mode operation.

Description :

The GLT41316 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41316 offers Fast Page mode ,and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{WE}$ pins. The GLT41316 has symmetric address and accepts 256-cycle refresh in 4ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256x16 bits, within a page, with cycle times as short as 18ns.

The GLT41316 is best suited for graphics, and DSP applications requiring high performance memories.

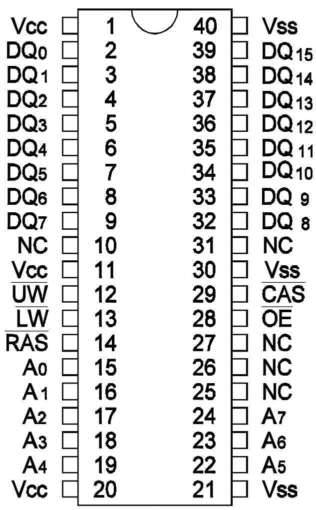
HIGH PERFORMANCE	**30**	**35**	**40**	**45**
Max. $\overline{RAS}$ Access Time, (t_{RAC})	30 ns	35 ns	40 ns	45 ns
Max. Column Address Access Time, (t_{AA})	15 ns	18 ns	20 ns	22 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	18 ns	21 ns	23 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	75 ns	80 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	10 ns	11 ns	12 ns	12 ns

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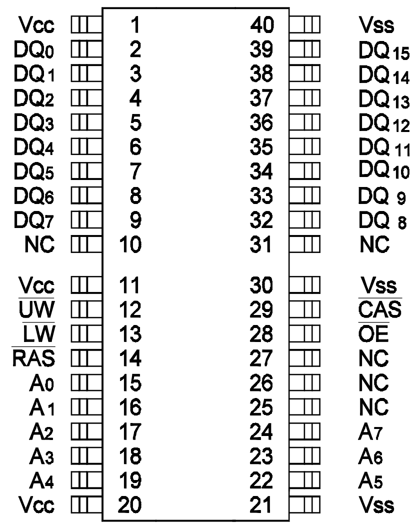
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Hsin Chu, Taiwan, R.O.C.

Pin Configuration :

GLT41316
SOJ Top View



TSOP(Type II)
Top View



Pin Descriptions:

Name	Function
A_0 - A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read / Upper Byte Write Enable
$\overline{LW}$	Read / Lower Byte Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_{15}	Data Inputs / Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient) ....-0°C to +70°C

Storage Temperature(plastic)....-55°C to +150°C

Voltage Relative to V_{SS}...............-1.0V to + 7.0V

Short Circuit Output Current......................50mA

Power Dissipation.....................................1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=5V±10%, V_{SS}=0V

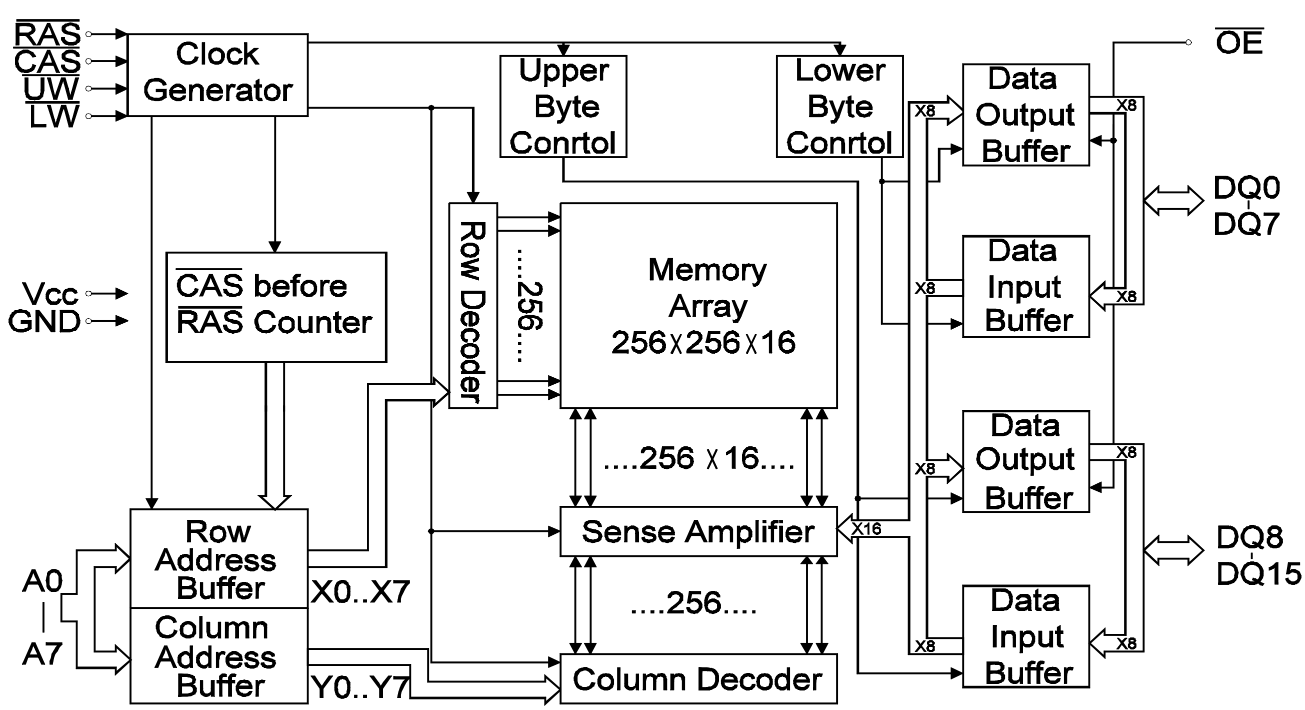
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{WE}$ means $\overline{UW}$ and $\overline{LW}$.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT41316

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$	$\overline{OE}$	ADDRESS	DQs	Notes
Standby		H	H→X	X	X	X		High-Z	
Read: Word		L	L	H	H	L	ROW/COL	Data Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	L	L	H	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
Fast-Page-Mode Read	1st Cycle	L	H→L	H	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L		H	L	COL	Data-Out	1
Fast-Page-Mode Write	1st Cycle	L	H→L	L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	L	L	X	COL	Data-In	2
Fast-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	H	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
$\overline{RAS}$ -Only Refresh		L	H	X	X	X	ROW	High-Z	
CBR Refresh		H→L	L	X	X	X		High-Z	

Notes:

1. These READ cycles are always WORD READ cycles .
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{UW}$ or $\overline{LW}$ active).
3. EARLY WRITE only.

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test=0V)		-10		+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ 5.5V Output is disabled (Hiz)		-10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥V_{SS}				4	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{RAS}$ cycling, $\overline{CAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC}(min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} (min.)	t_{RAC} = 30ns t_{RAC} = 35ns t_{RAC} = 40ns t_{RAC} = 45ns			180 170 160 150	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{CAS}$ ≥V_{CC}-0.2V, All other inputs ≥V_{SS}				2	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		V_{CC}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5mA		2.4			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC(max.)}$ is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified $I_{CC(max.)}$ is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
3. Specified $V_{IL(min.)}$ is steady state operation. During transitions $V_{IL(min.)}$ may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with $V_{IL(min.)}$≥V_{SS} and $V_{IH(max.)}$≤V_{CC}.

AC Characteristics ($0^{\circ}C \leq T_A \leq 70^{\circ}C$, See note 1,2)

Test condition: V_{CC}=5.0V±10%, V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.4V/0.4V

Parameter	Symbol	t_{RAC} = 30 ns		t_{RAC} = 35 ns		t_{RAC} = 40 ns		t_{RAC} = 45 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	65	-	70	-	75	-	80	-	ns	
Read Midify Write Cycle Time	t_{RWC}	80	-	99	-	105	-	110	-	ns	
Access Time from $\overline{RAS}$	t_{RAC}	-	30	-	35	-	40	-	45	ns	3,4
Access Time from $\overline{CAS}$	t_{CAC}	-	10	-	11	-	12	-	12	ns	3,4
Access Time from Column Address	t_{AA}	-	15	-	18	-	20	-	22	ns	3,4
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0		0	-	0	-	0	-	ns	3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFF}	3	8	3	8	3	8	3	8	ns	7
Transition Time(Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	25	-	25	-	25	-	25	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	30	100k	35	100k	40	100K	45	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	-	12	-	12	-	13	-	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	30	-	36	-	40	-	46	-	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10000	12	10000	12	10000	13	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	13	20	17	24	18	28	18	33	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	10	15	12	17	13	20	13	23	ns	4
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	-	5	-	5	-	5	-	ns	8
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	7	-	7	-	8	-	8	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	6	-	6	-	6	-	6	-	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	26	-	30	-	34	-	39	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	15	-	18	-	20	-	23	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	0	-	ns	9
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	0	-	ns	9
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	6	-	6	-	6	-	6	-	ns	10
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	26	-	30	-	34	-	39	-	ns	5
$\overline{WE}$ Pulse Width	t_{WP}	6	-	6	-	6	-	6	-	ns	10

Parameter	Symbol	t_{RAC} = 30 ns		t_{RAC} = 35 ns		t_{RAC} = 40 ns		t_{RAC} = 45 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	-	11	-	12	-	12	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	-	11	-	12	-	12	-	ns	
Data-In Setup Time	t_{DS}	0	-	0	-	0	-	0	-	ns	11
Data-In Hold Time	t_{DH}	7	-	7	-	8	-	8	-	ns	11
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	27	-	31	-	36	-	41	-	ns	6
$\overline{WE}$ Setup Time	t_{WCS}	0	-	0	-	0	-	0	-	ns	5
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	47	-	58	-	63	-	68	-	ns	5
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	24	-	29	-	30	-	30	-	ns	5
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	29	-	36	-	38	-	40	-	ns	5
$\overline{CAS}$ Setup Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5	-	5	-	5	-	5	-	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	-	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5	-	5	-	5	-	5	-	ns	
$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	t_{CPT}	20	-	20	-	20	-	20	-	ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	-	18	-	21	-	23	-	25	ns	3
Fast Page mode Read/Write Cycle Time	t_{PC}	18	-	21	-	23	-	25	-	ns	
Fast Page mode Read Modify Write Cycle Time	t_{PRWC}	48	-	60	-	63	-	65	-	ns	
$\overline{CAS}$ Precharge Time(Fast Page mode)	t_{CP}	5.5	-	6	-	7	-	7	-	ns	
$\overline{RAS}$ Pulse Width(Fast Page mode)	t_{RASP}	30	100k	35	100k	40	100K	45	100K	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	25	-	25	-	25	-	30	-	ns	
Access Time from $\overline{OE}$	t_{OEA}	-	10	-	11	-	12	-	12	ns	
$\overline{OE}$ to Delay Time	t_{OED}	8	-	8	-	8	-	8	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	3	8	3	8	3	8	3	8	ns	7
$\overline{OE}$ Hold Time	t_{OEH}	6	-	6	-	7	-	7	-	ns	
$\overline{WE}$ Hold Time(Hidden Refresh Cycle)	t_{WHR}	15	-	15	-	15	-	15	-	ns	
Refresh Time(256cycles)	t_{REF}	-	4	-	4	-	4	-	4	ms	

Notes

1. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh cycles to initialize the internal circuit.

2. $V_{IH(min.)}$ and $V_{IL(min.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$, AC measurements assume t_T = 3ns.

3. Measured with an equivalent to 2 TTL loads and 100pF.

4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

5. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min.)}$,$t_{RWD} \geq t_{RWD\ (min.)}$ and $t_{AWD} \geq t_{AWD(min.)}$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

6. t_{AR}, t_{WCR}, and t_{DHR} are referenced to $t_{RAD(max.)}$.

7. $t_{OFF(max.)}$ and $t_{OEZ(max.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

8. $t_{CRP(min)}$ requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycle preceded by any cycles.

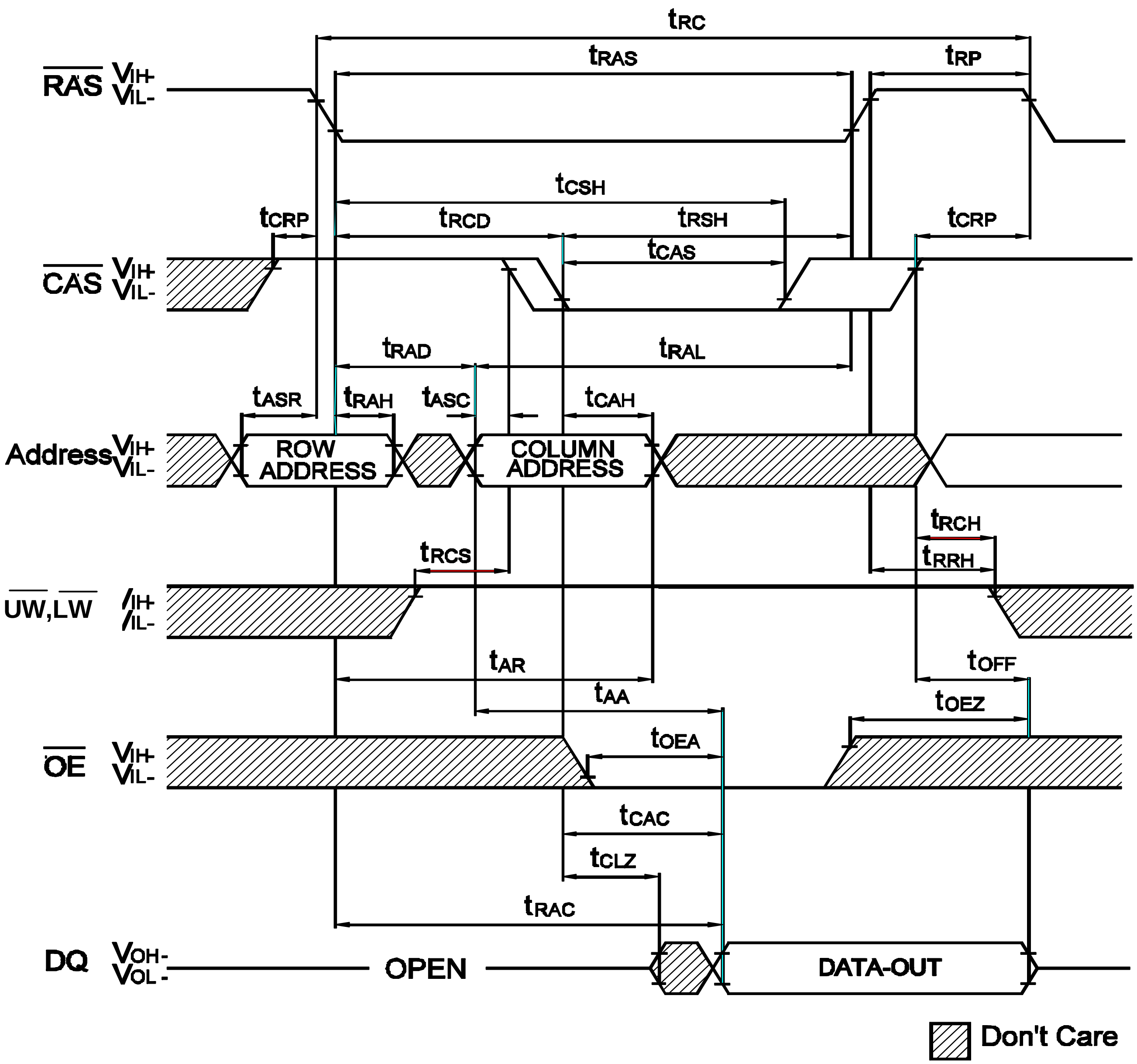
9. Either $t_{RCH(min.)}$ or $t_{RRH(min.)}$ must be satisfied for a read cycle.

10. $t_{WP(min.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH(min.)}$ should be satisfied.

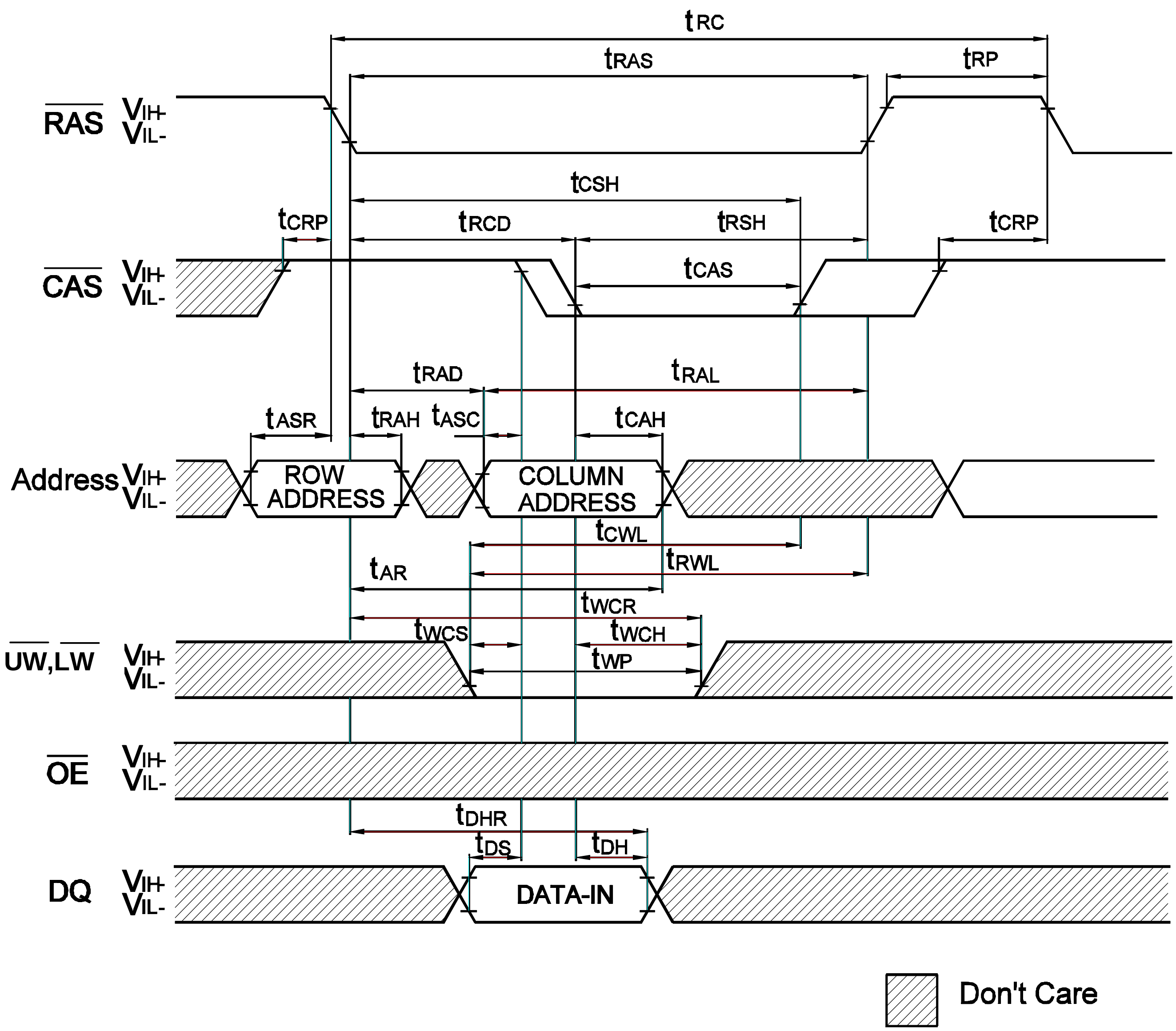
11. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.

Read Cycle

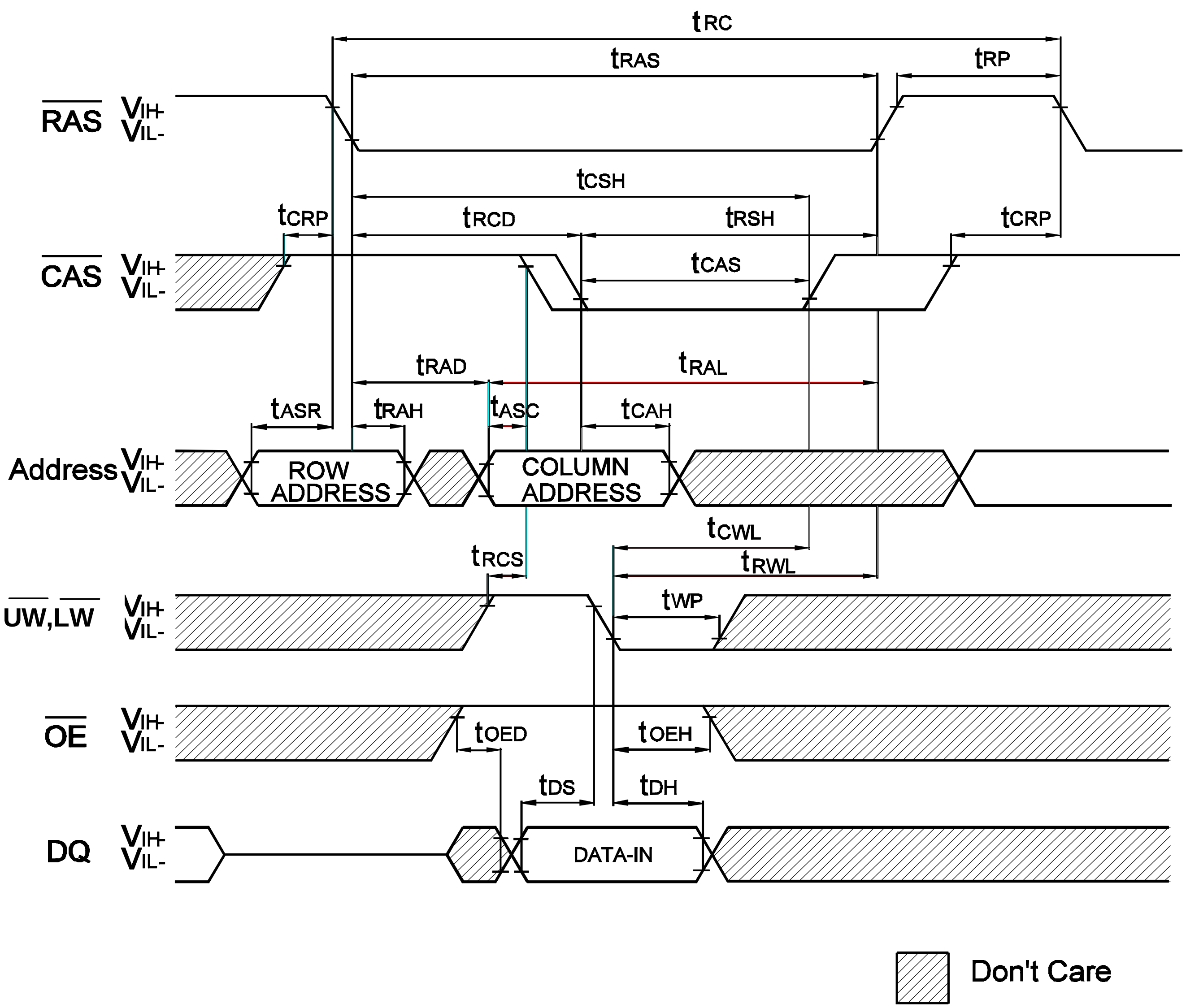
Note : D_{IN} = OPEN



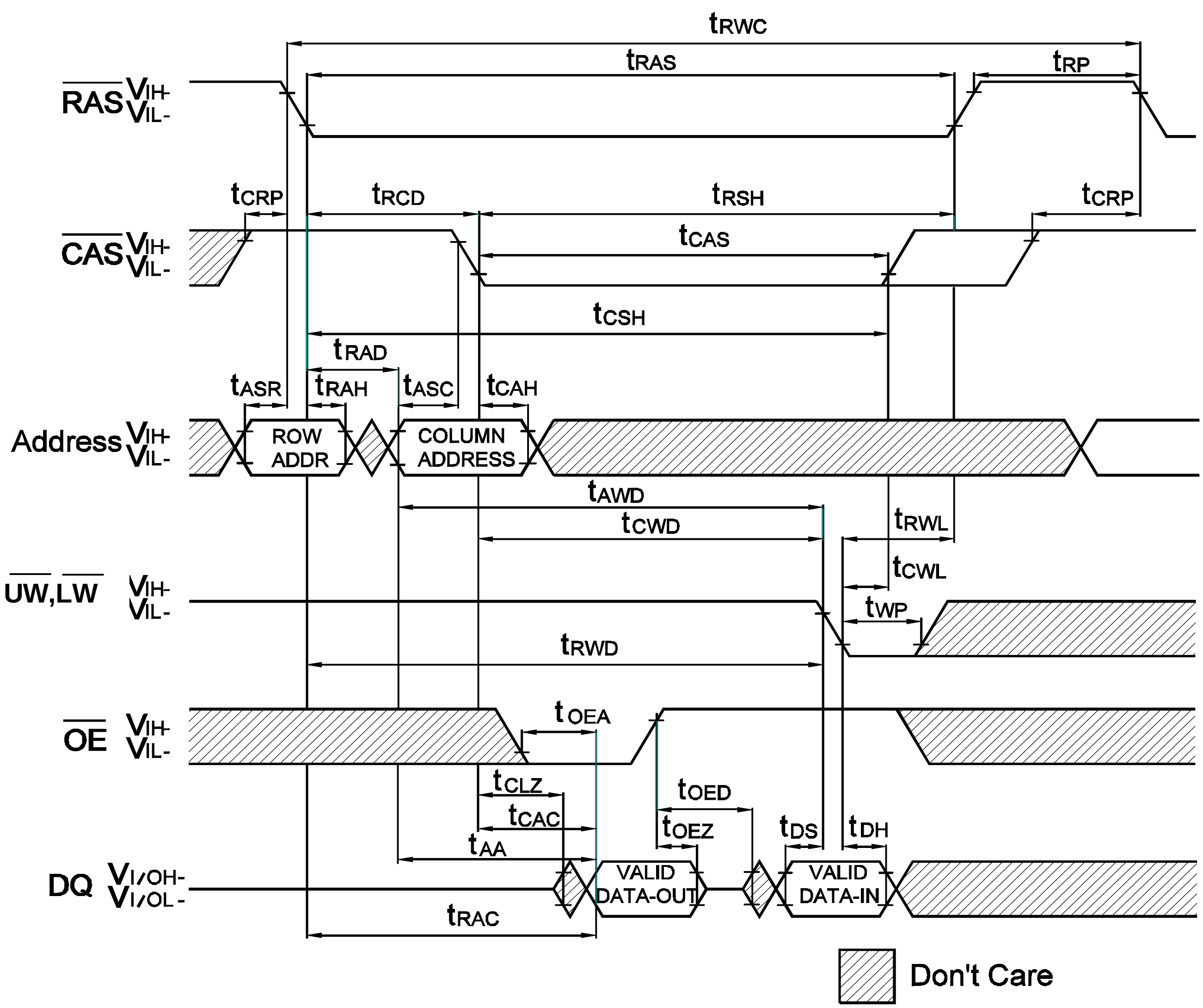
Early Write Cycle
NOTE : D_{OUT} = OPEN



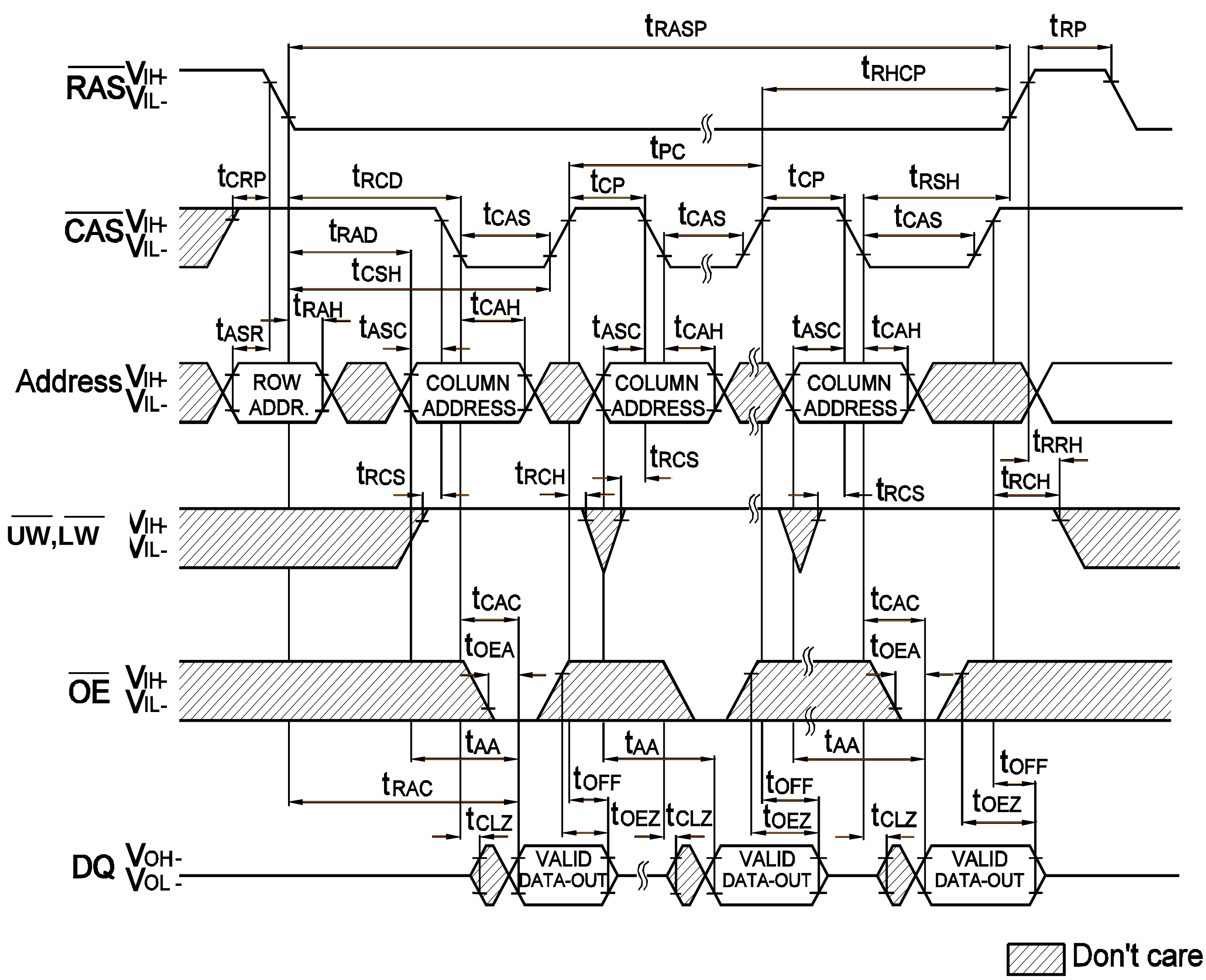
Late Write Cycle ($\overline{OE}$ Controlled Write)
NOET : D_{OUT} = OPEN



Read - Modify - Write Cycle

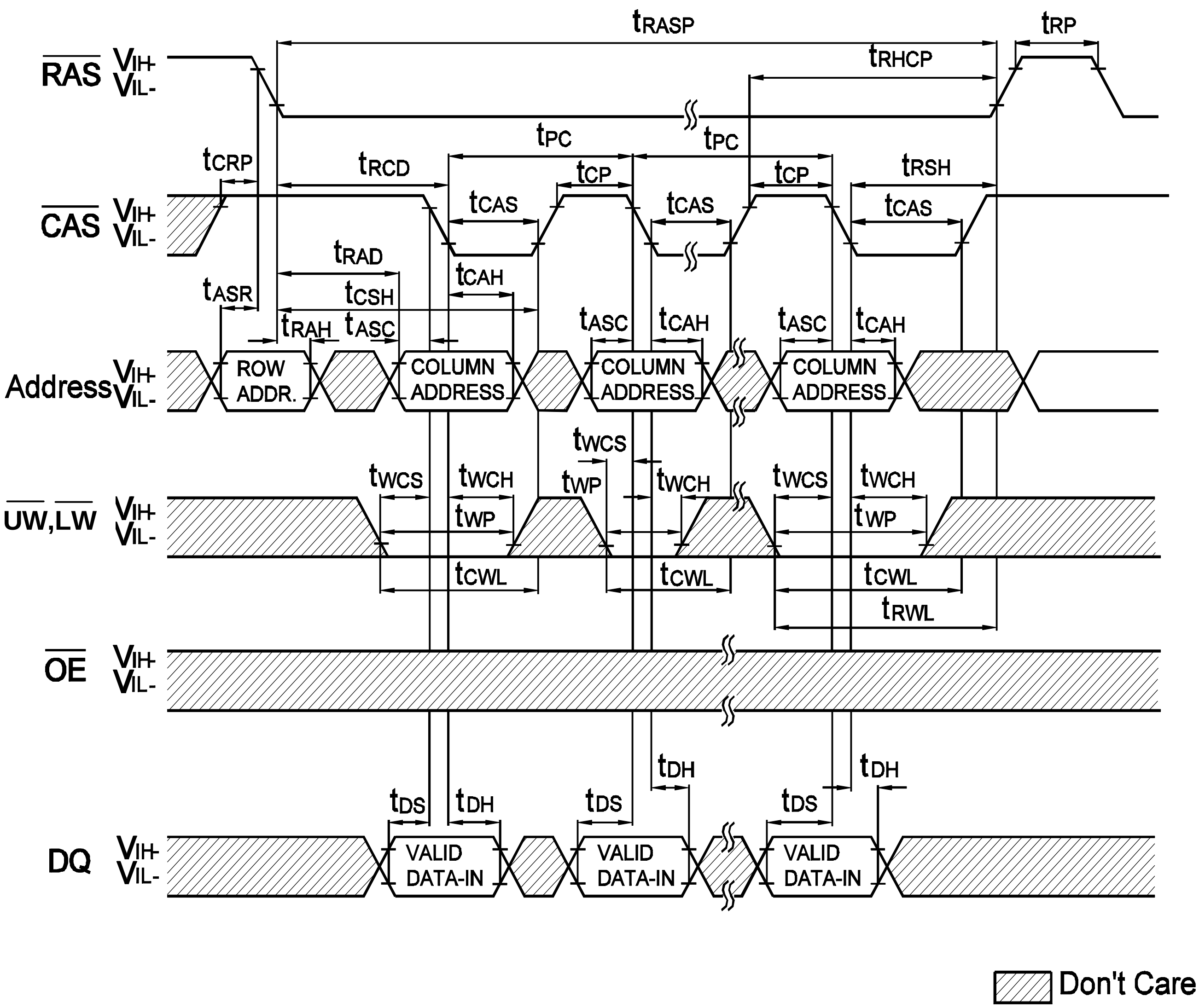


Fast Page Read Cycle

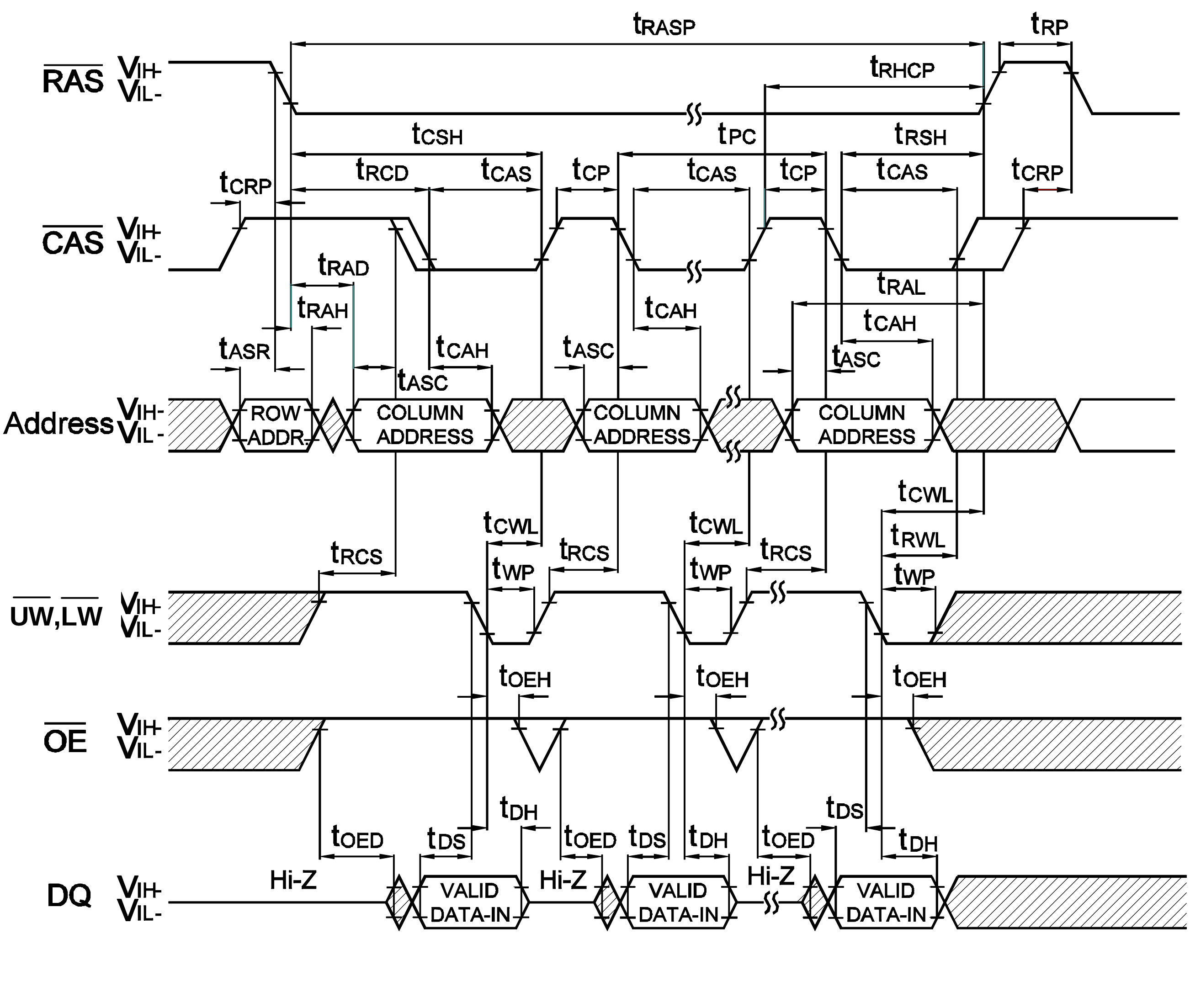


Fast Page Early Write Cycle

NOTE : D_{OUT} = OPEN

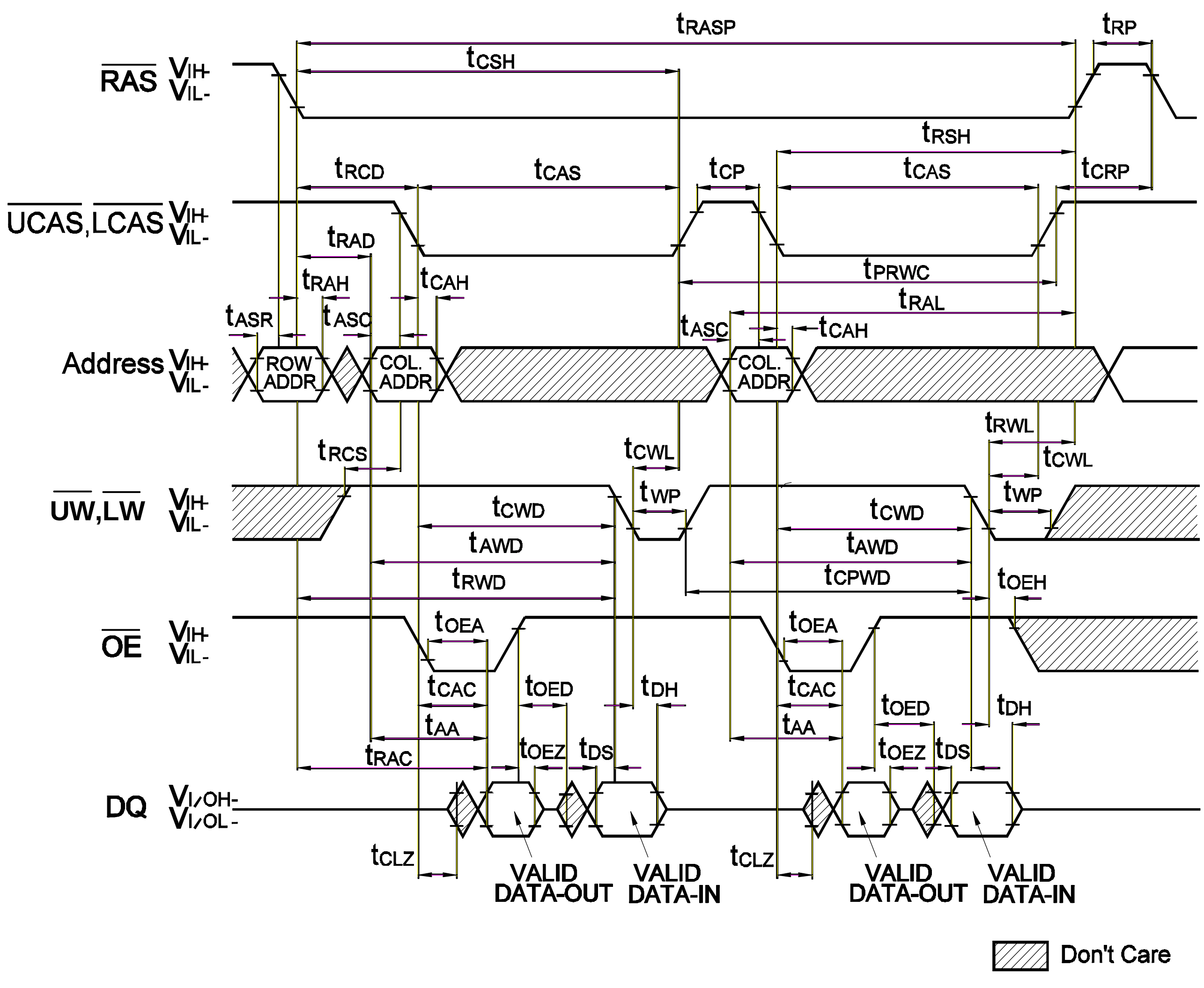


Fast Page Mode Late Write Cycle

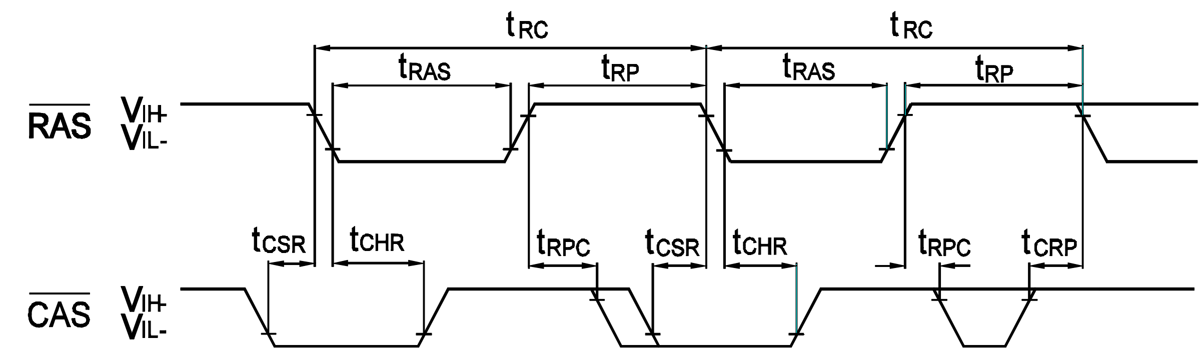


Fast Page Read-Modify-Write Cycle

NOTE : D_{OUT} = OPEN

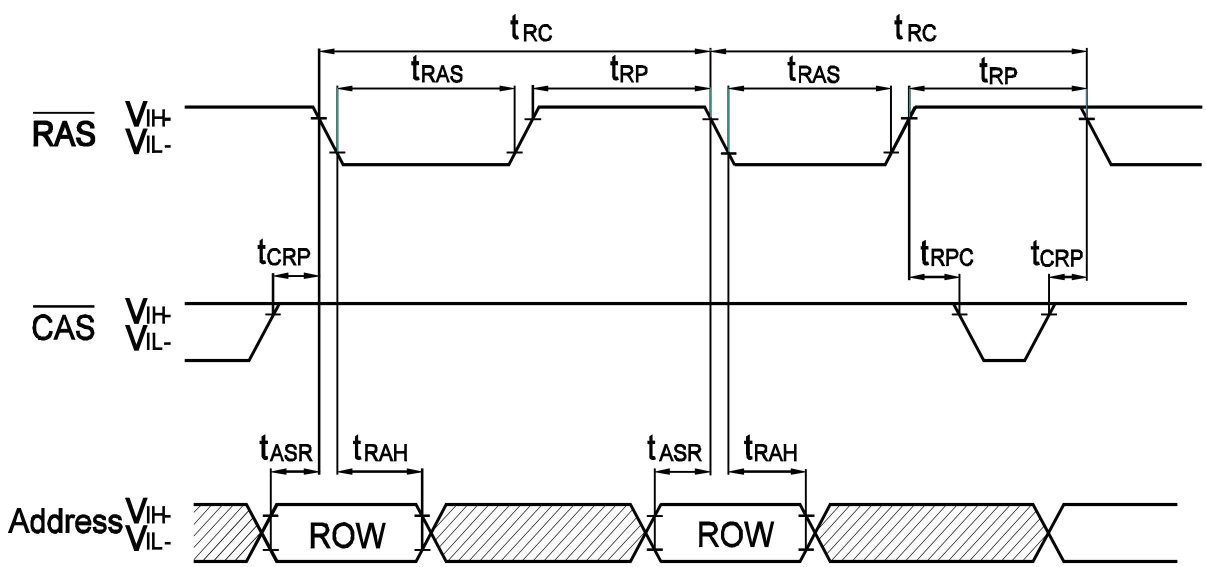


$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



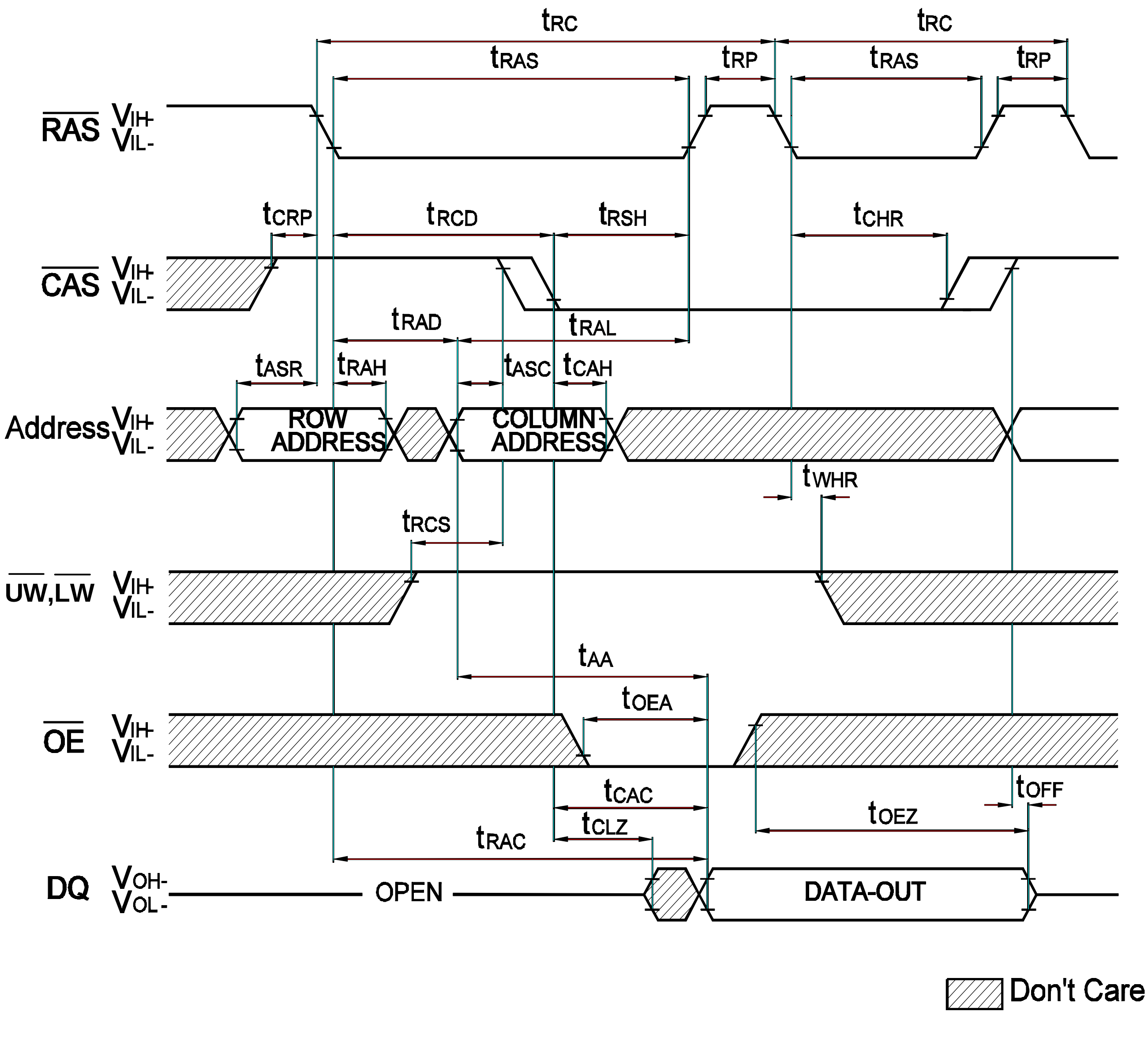
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care DQ : Hi - Z

$\overline{\text{RAS}}$-Only Refresh Cycle

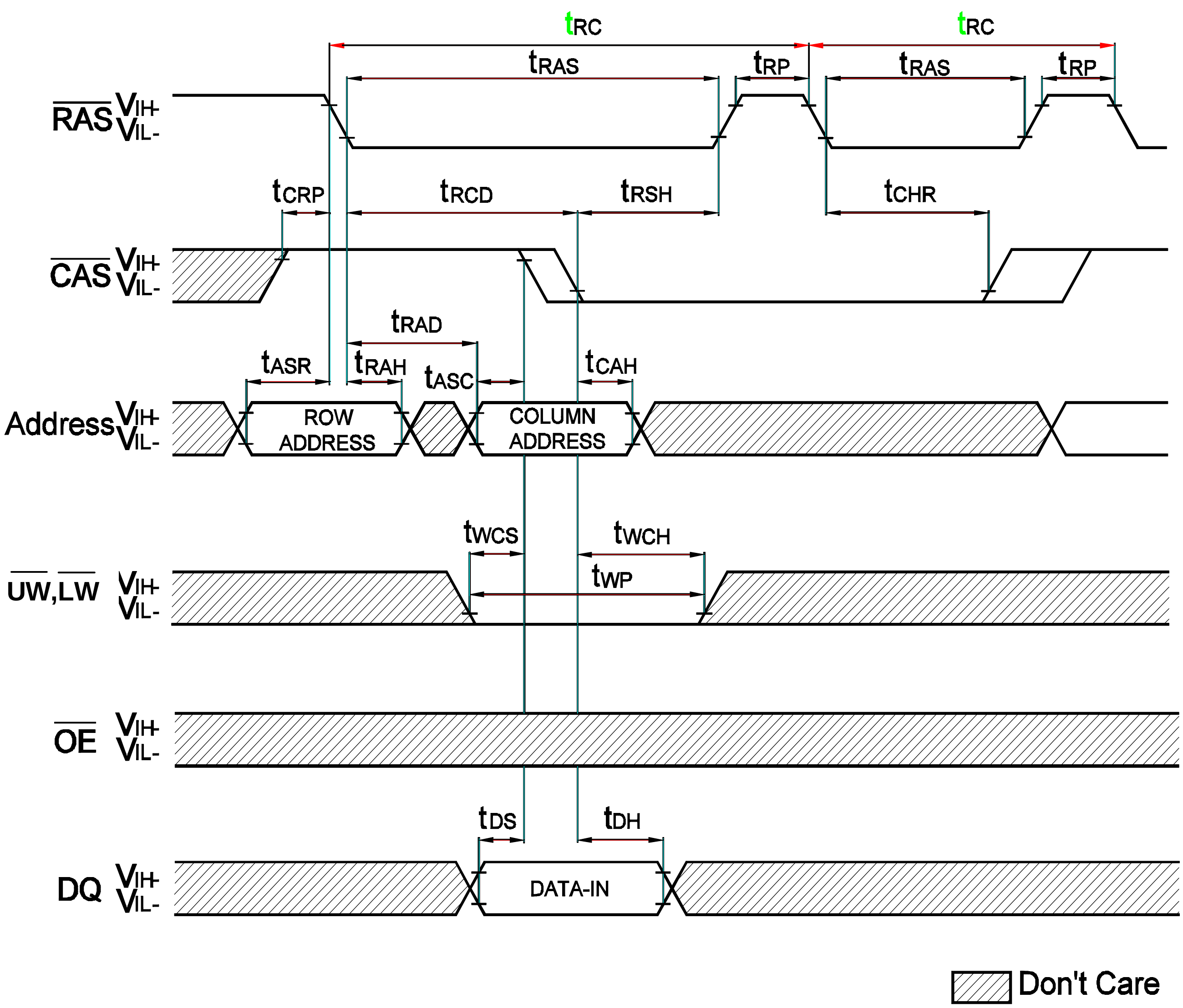


Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care DQ : Hi - Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)
NOTE : D_{OUT} = OPEN



Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*PACKAGE*
GLT41316-30J4	30ns	Normal	FPM	SOJ 400mil 40L
GLT41316-35J4	35ns	Normal	FPM	SOJ 400mil 40L
GLT41316-40J4	40ns	Normal	FPM	SOJ 400mil 40L
GLT41316-45J4	45ns	Normal	FPM	SOJ 400mil 40L
GLT41316-30TC	30ns	Normal	FPM	TSOP 400mil 44L
GLT41316-35TC	35ns	Normal	FPM	TSOP 400mil 44L
GLT41316-40TC	40ns	Normal	FPM	TSOP 400mil 44L
GLT41316-45TC	45ns	Normal	FPM	TSOP 400mil 44L

Parts Numbers (Top Mark) Definition :

GLT 4 13 _ 16 - 40 J4

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : Mix Voltage

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

SPEED
-SRAM
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

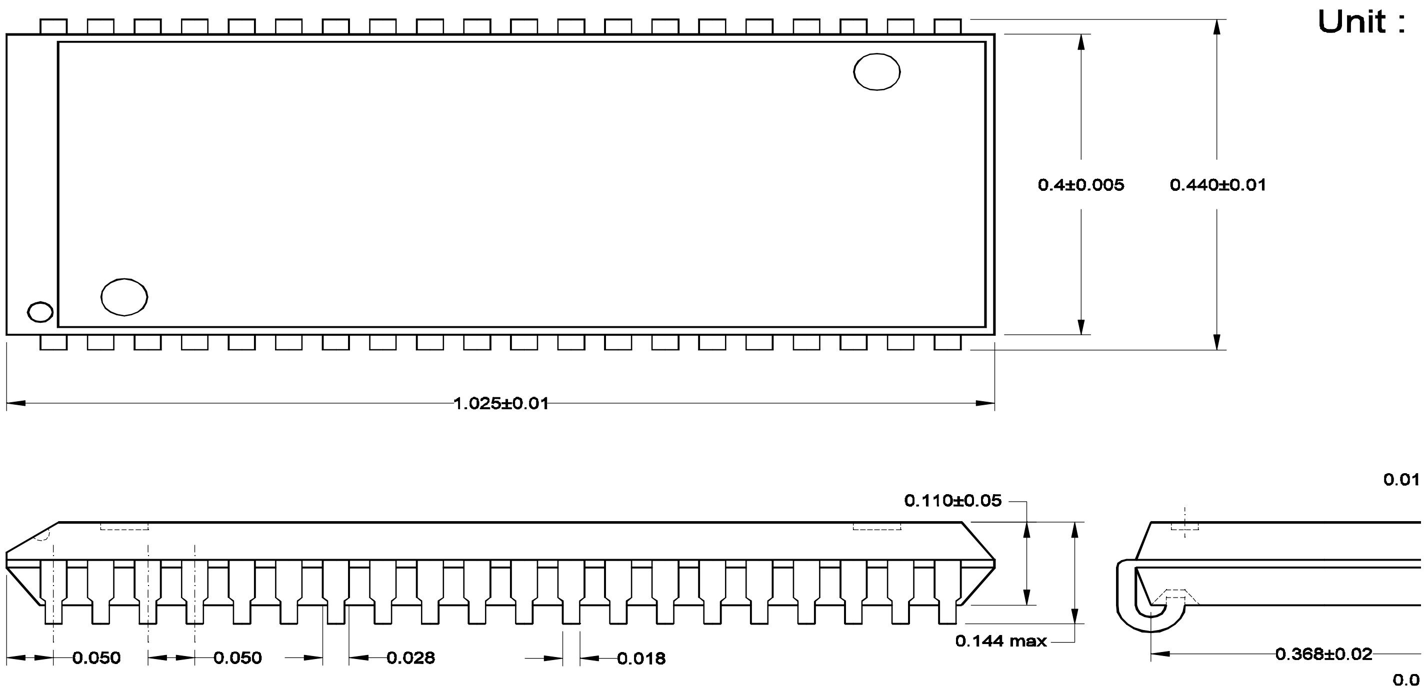
Note : C→CDROM , H→HDD.

Example :

1.GLT710008-15T   1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4   4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

400mil 40 pin Small Outline J-form Package (SOJ)



40/44 Lead Thin Small Outline Package TSOP(Type II)

